Silicon Tracker Status Report

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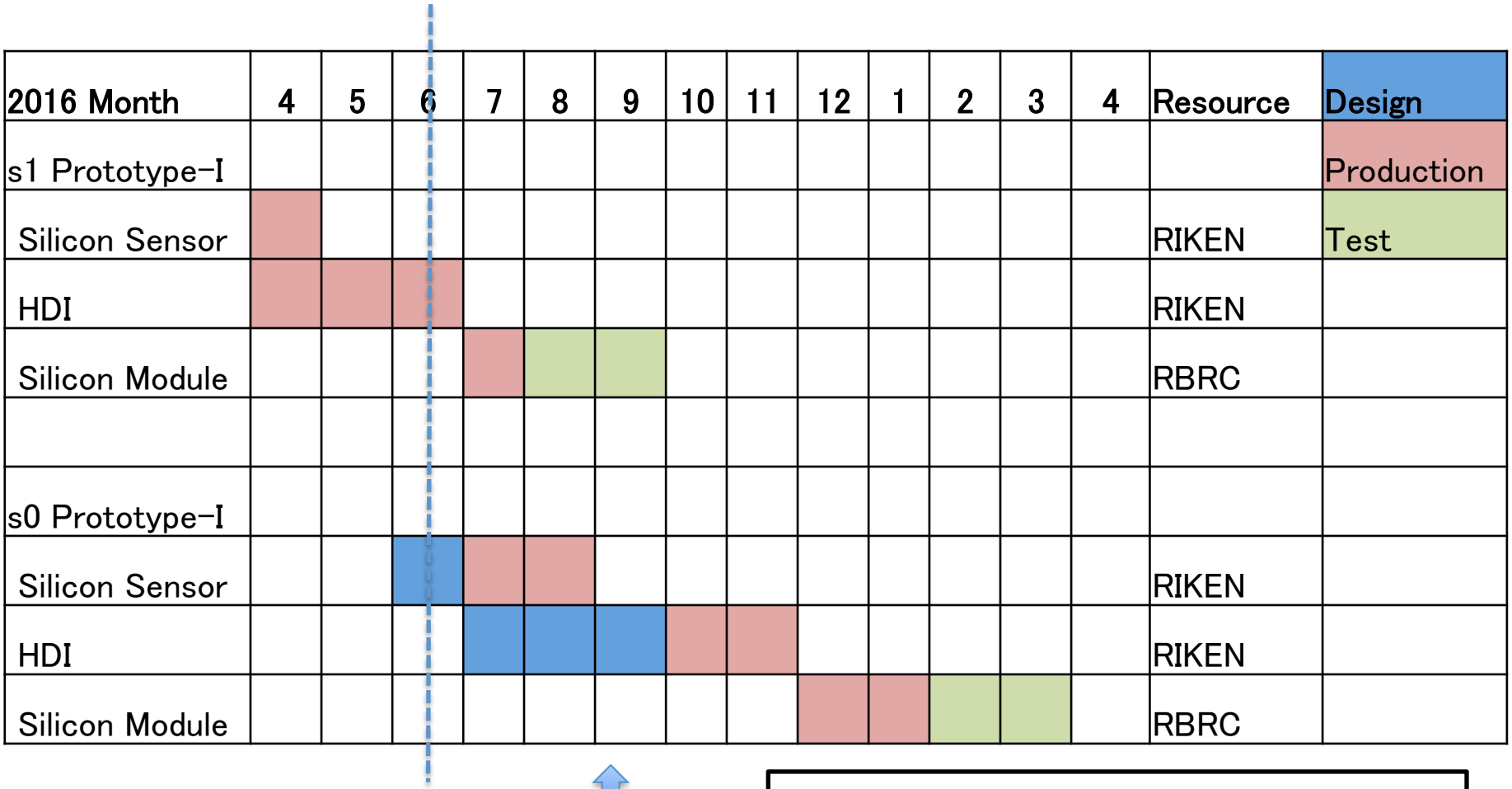
for the Silicon Tracker Group

Plan for JFY2016



s1 development and s0 R&D will be reported in the review in addition to simulation work for the performance.

s1 prototype

- s1 prototype became out of use now though, we still continue assembly for following purpose:

1. Setup the test bench for testing with up-to-date readout system which is valid for next decade.
2. Check the electrical layout is correct
3. Layer structure is also OK
4. Cooling capability

Cooling Option

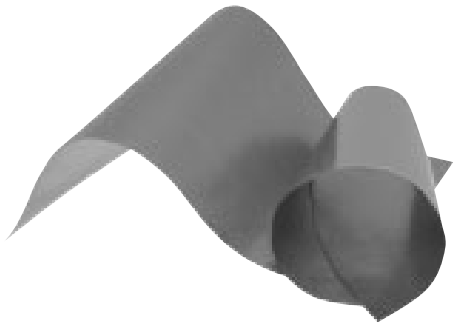
- In addition to air cooling option, the high thermal conductivity plate (sheet) will be tested. It has an advantage to make the cooling system even simpler and less material.

Panasonic "PGS" Graphite Sheets

"PGS" Graphite Sheets

Type: **EYG**

PGS (Pyrolytic Graphite Sheet) is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a higly oriented graphite polymer film. It is ideal for providing thermal management/heat-sinking in limited spaces or to provide supplemental heat-sinking in addition to conventional means. This material is flexible and can be cut into customizable shapes.



■ Characteristics

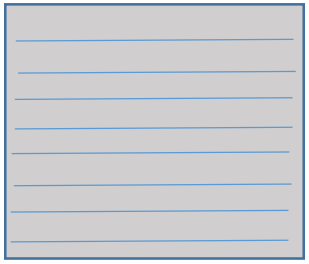
Characteristics		Specification	Specification	Specification
Thickness		0.10 ± 0.03 mm	0.07 ± 0.015 mm	0.025 ± 0.010 mm
Density		0.85 g/cm^3	1.1 g/cm^3	2.1 g/cm^3
Thermal conductivity	a-b plane	600 to 800 W/(m·K)	750 to 950 W/(m·K)	1500 to 1700 W/(m·K)
Electrical conductivity		10000 S/cm	10000 S/cm	20000 S/cm
Extensional strength		19.6 MPa	22.0 MPa	30.0 MPa
Expansion coefficient	a-b plane	9.3 × 10^{-7} 1/K	9.3 × 10^{-7} 1/K	9.3 × 10^{-7} 1/K
	c axis	3.2 × 10^{-5} 1/K	3.2 × 10^{-5} 1/K	3.2 × 10^{-5} 1/K
Heat resistance		400 °C		
Bending(angle 180,R5)		10000 cycles		

Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use.
Should a safety concern arise regarding this product, please be sure to contact us immediately.

00 Sep. 2008

s0 Sensor Design

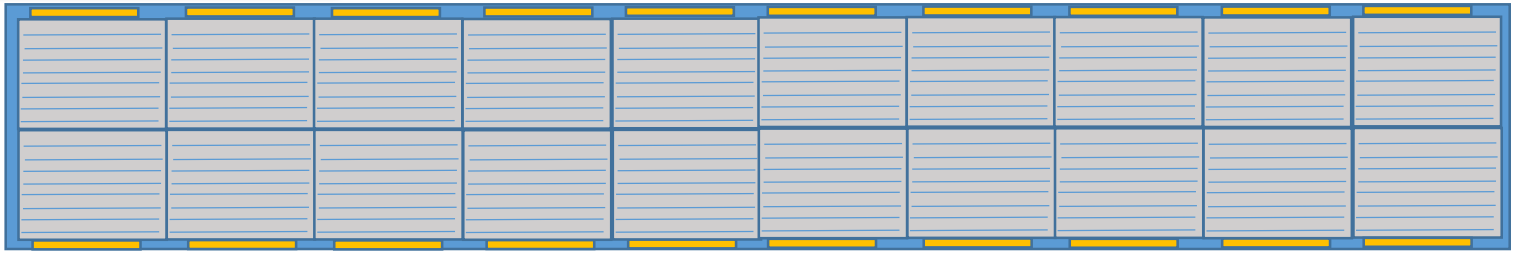
Silicon Cell



Number of Strips	**128**
Strip width	84 um
Strip length	12 mm

Block Width	**128 × 84 um = 10.752 mm**
Block Length	12 mmm

Silicon Sensor



Number of Blocks	**12 × 2 =34**
Active Are	(2 × 10.752) mm × (12 × 10) mm

Design by Yasuyuki Akiba

s0 sensor prototype

- First discussion with Hamamatsu on May 26 about the concept.
- Design work requested to Hamamatsu
- Next meeting is scheduled in July 20th, hoping the design work is in a reasonable shape by then at least for the first round.
- Consulting with Hamamatsu if the current design can fit 4 s0 sensors/wafer.

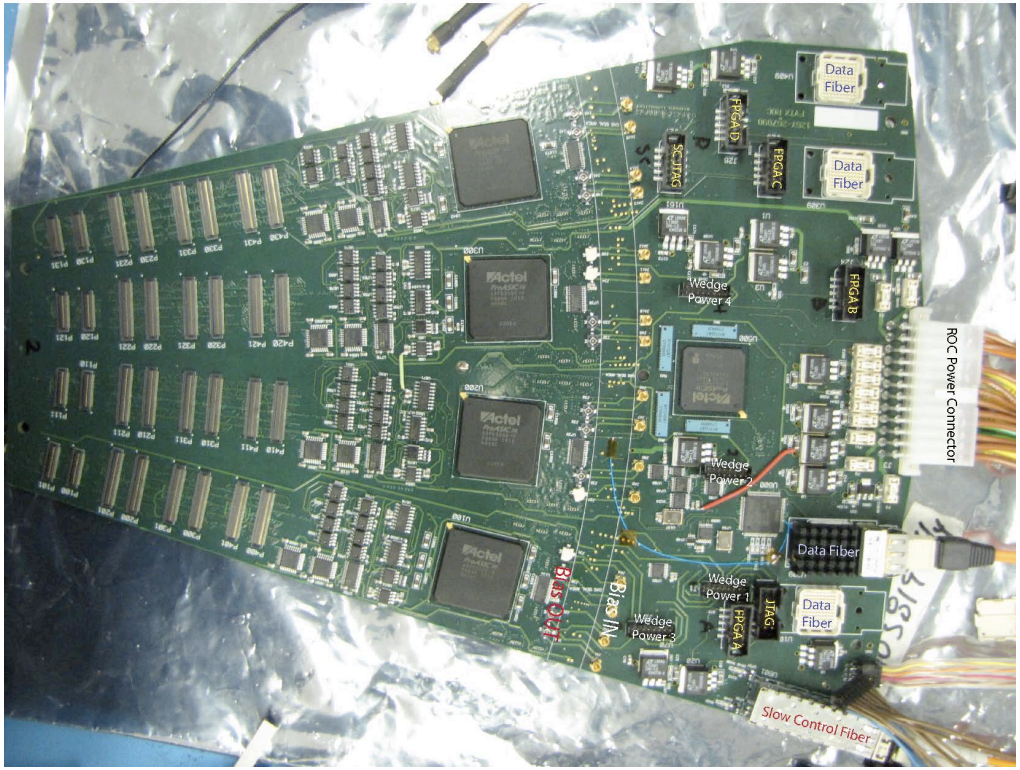
s0 HDI design

- Start action from next week.
- Even compact size and higher density than the s1 HDI is required.
- Will discuss the feasibility with Yamashita Co.
- In addition, we will consult with
  - Tokai Electronics (made pixel bus)
  - Taiyo Industrial Co (developing FPC for KEK)

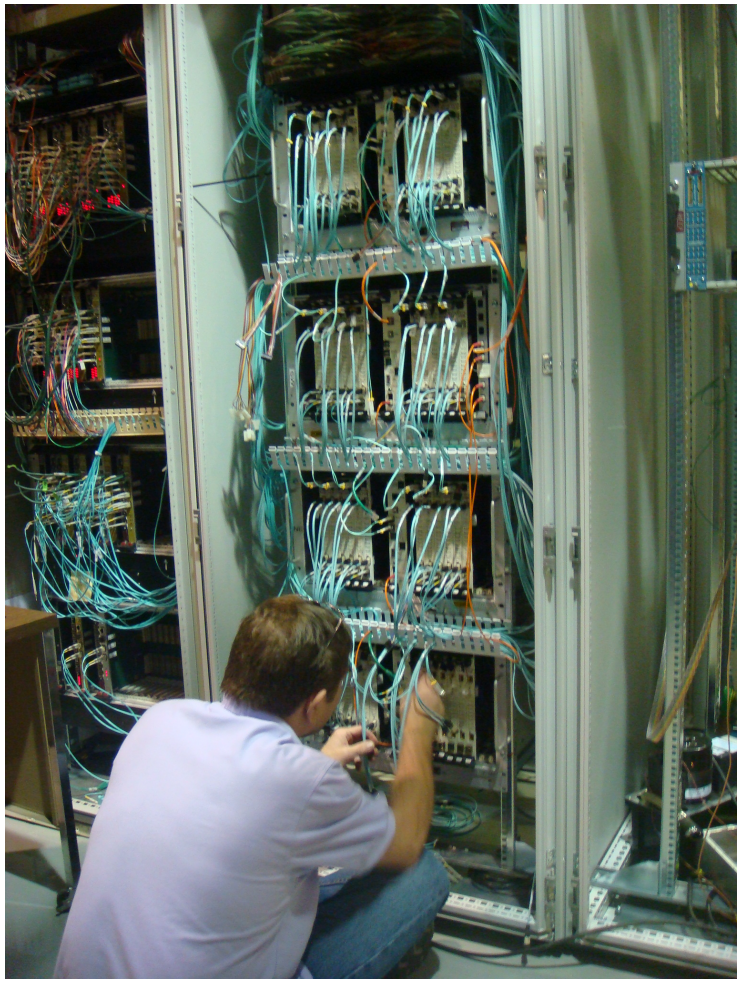
Reuse FVTX Readouts for s0

- We are seeking for the s0 silicon sensors to reuse the FVTX electronics by introducing some sort of adapter to fit to the FVTX ROC design.
- FVTX ownership will be transferred from LANL to BNL after Run16. We arranged all electronics to be kept in (F)VTX test bench area in BNL until we give up the design for reuse.

FVTX Readout Electronics

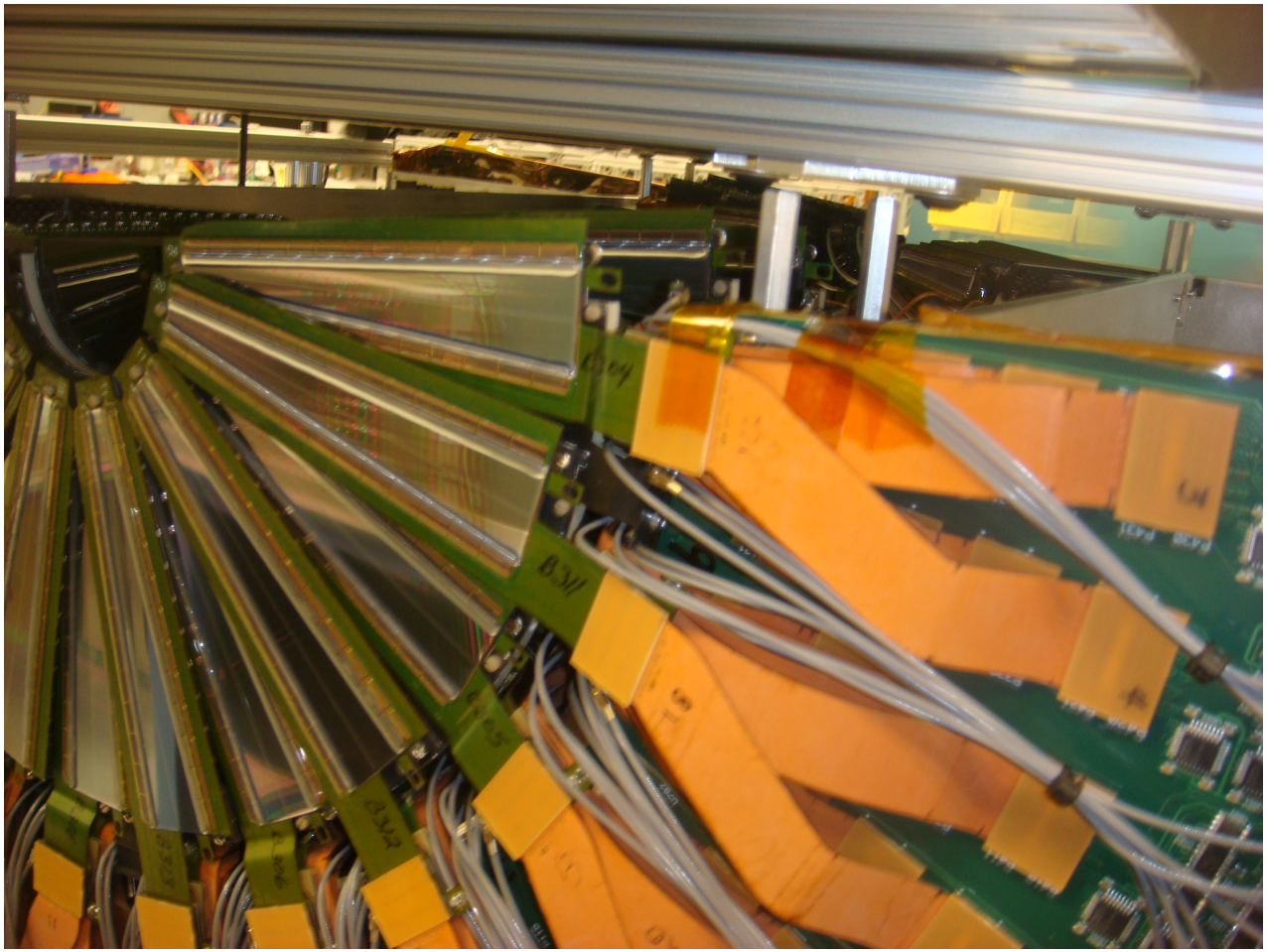


ROC



FEM - FEMIB

Compatibility



We may need to develop the adapter for s0 ladder HDIs to fit to the ROC input connector geometry.

Summary

- We will continue testing s1 sensor modules for test bench warm up, cooling, etc.
- s0 sensor design discussion had started with Hamamatsu
- s0 HDI R&D will be started soon.
- Reserved FVTX readout electronics for reuse.